

## MULTIPLEXER DATA ACQUISITION SYSTEM

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### MULTIPLEXERS GENERATE STEEP SIGNAL EDGES AND TRANSPORT THE CHARGE

Multiplexers have been used for acquisition of quasi-static signals for a long time. While these signals usually have a low bandwidth of only a few hertz, applications generally require that the multiplexer send each signal as fast as possible to the converter and that the signals be processed quickly. To ensure fast processing, such acquisition systems usually include a sense amplifier behind the multiplexer to adjust the signal level to the analog-to-digital converter and to prevent current caused by the signals coming from the multiplexer. But as common as this configuration is today, it still produces unexpected errors again and again.

Unless the multiplexer is driven in low-impedance mode or from a capacitive source, charge transmission from one channel to another can be expected. Errors the size of several LSBs of a 12-bit converter can arise, especially in passive low-pass circuits in front of the input, such as those used for EMC rejection, ESD, and overvoltage protection.

Besides leakage currents, which are very small in modern designs, important factors are the switching of the multiplexer output capacitance and of the input current from the succeeding sense amplifiers, which are usually dynamically overloaded at the time of switching.

### DYNAMIC OVERLOAD

Multiplexers switch from one channel to the next in a few nanoseconds. This switching produces a correspondingly steep signal pulse for the succeeding sense amplifier. This steep edge, however, is only compensated by feedback amplifiers after the settling time has finished. Using the example of an op amp, this process is easy to explain.

Settling time with an op amp: there is +10V at channel 1 and 0V at channel 2 (see Figure 2). The switching produces a voltage step from 10V to 0V. The output of the op amp also goes from 10V to 0V in a few microseconds, depending upon the slew rate. Meanwhile, a stress flow arises at the input with a peak value of 10V since the feedback input of the op amp is connected to the output.

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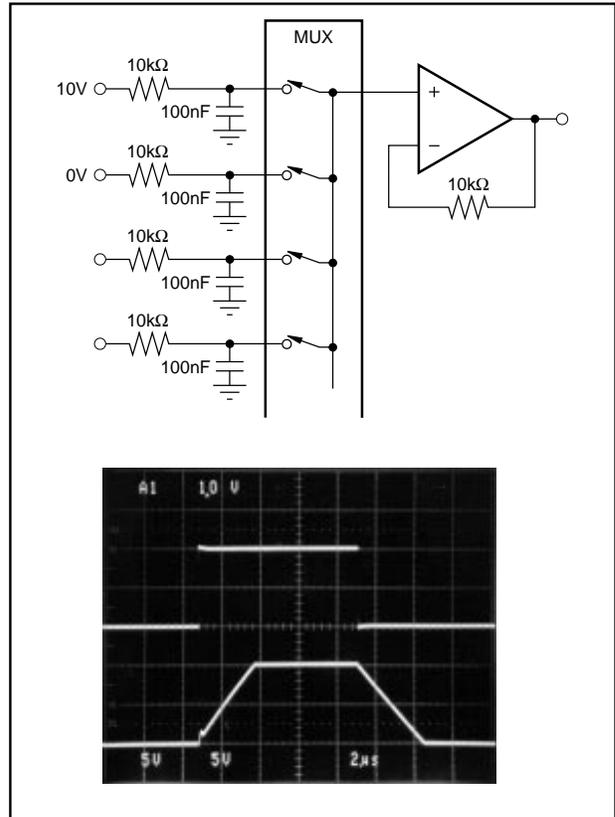


FIGURE 1. Step Response of Single-Ended Multiplexer, Switching Between 0V and +10V.

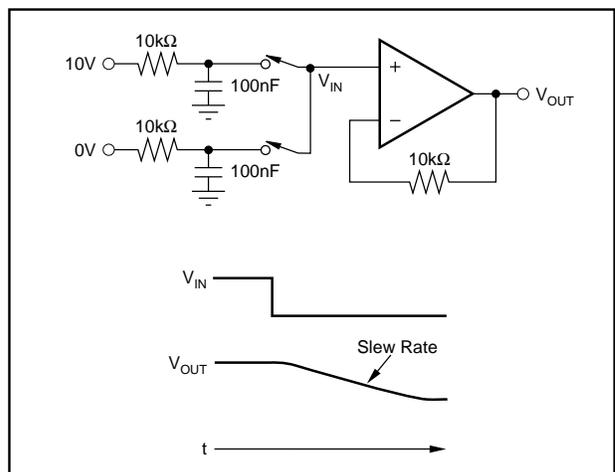


FIGURE 2. Overload of the Op Amp Caused by Fast Switching.

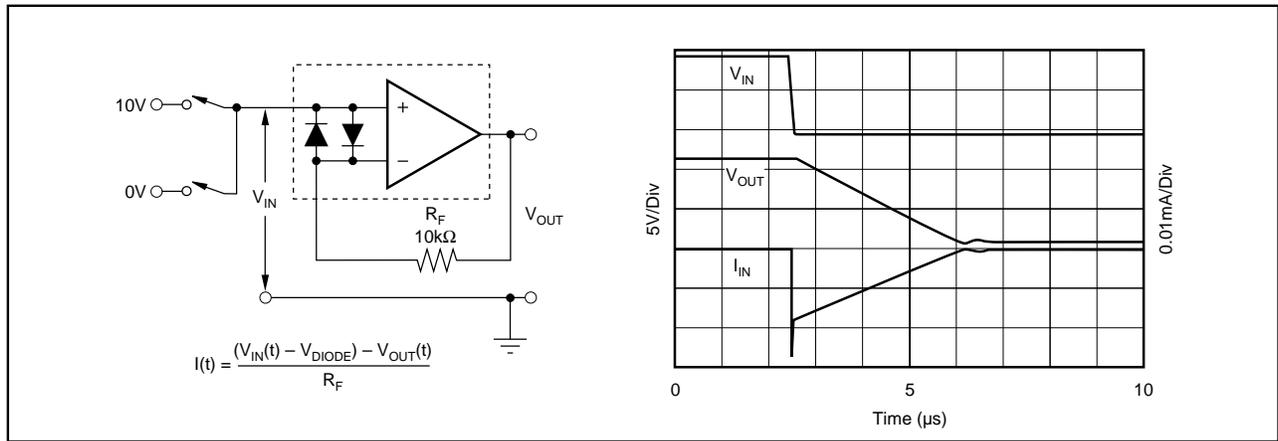


FIGURE 3. An Input Current Flows Through the Protection Diodes and  $R_F$ .

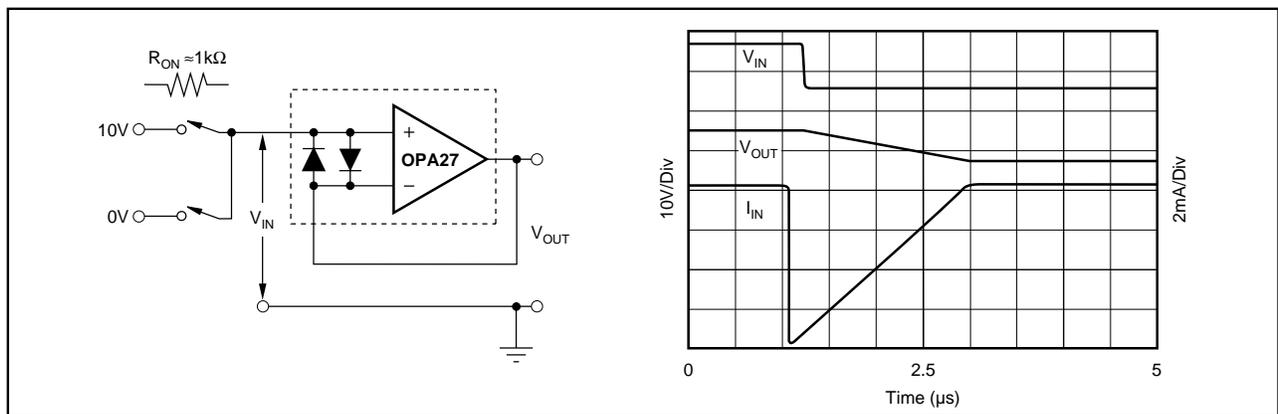


FIGURE 4. No Current Limitation Can Lead to Destruction of the OPA27.

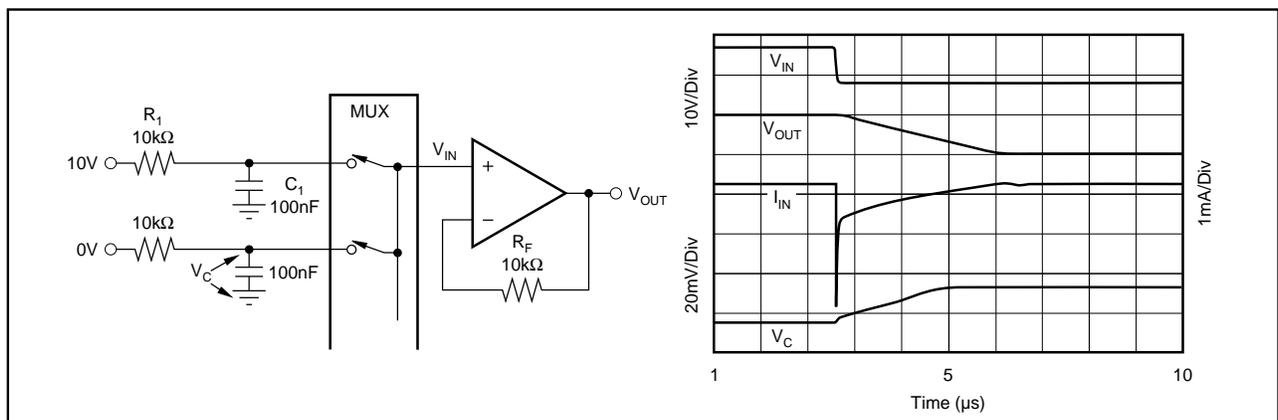


FIGURE 5. Changing the Charge in the 100nF Capacitor.

Since 10V of voltage difference between the inputs would damage bipolar op amps, protection diodes are generally located at the inputs. These protection diodes, with a clamp voltage of approximately 0.7V, prevent a rise in voltage in case of overload. As a consequence, however, a current flows from the noninverting input via this protection circuitry to the inverting input and from there to the output of the op amp (see Figure 3).

The current is limited by the source, as well as by  $R_F$  or the short-circuit current of the op amp. When  $R_F = 10k\Omega$ , the resulting current is  $(10V - 0.7V)/10k\Omega < 1mA$ . If  $R_F$  and the MUX channel resistor were not present, the 60mA output current of an OPA27 would already damage the input, as illustrated in Figure 4. In practice, the current is also limited

by the on-resistance of the multiplexer, which can vary between several ohms and several kilo ohms, depending upon the type. If a filter capacitor is located in front of the multiplexer, it functions as a low-impedance voltage source. Figure 5 shows the measurements from this configuration.

It is interesting to note that this current can only flow into the input stage because of the protection circuitry of the bipolar transistors. In FET op amps, this protection is not necessary and consequently no current flows out of the signal source. Comparing the input circuits of bipolar and FET op amps clearly illustrates this distinction. While the transistor's reversed base-emitter junction breaks at about 7V, the blocked gate channel diode of a J-FET can handle more than 30V.

### CONSEQUENCES FOR THE INPUT FILTER

If a bipolar op amp is inserted after the multiplexer with preceding low-pass filter, the overload input current flows from the filter capacitor into the amplifier circuit, as shown in Figure 5. Here, a simple example shows the size of this error:

In the first approximation, the error current ( $I_N$ ) curve resembles a sawtooth shape. The peak value, as shown in Figure 5, is:

$$I_E = \frac{10V - 0.7V}{10k\Omega = 1.5k\Omega} \approx 0.8mA$$

The settling time should be about 3 $\mu$ s (linear ramp):

$$\Delta V_C = \frac{I \cdot t}{C \cdot 2} = \frac{0.8mA \cdot 3\mu s}{100nF \cdot 2} = 12mV$$

Therefore, the filter capacitor will change its voltage by 12mV with 3 $\mu$ s. This does not include the recharging current from the voltage via  $R_1$ . Note:  $\tau$  is the time constant for the time required to recharge the last charge. Unfortunately, however, this recharging current is almost neglectable because of the long time constant:

$$\tau = 10k\Omega \cdot 100nF = 1ms!$$

Thus, compensating for the initial droop would take a relatively long time.

As a result, the voltage difference of the channels switched one after another by the MUX produces a corresponding overload error current in the amplifier, which results in a lot of crosstalk.

### GAIN PERFORMANCE

The large current already mentioned also flows into or through the protection circuitry, especially at large signal levels. For this reason, the important factor is the voltage threshold of the protection diodes. At an input voltage of only 1V and a corresponding gain of 10V/V, the protection diodes are conductive only for a small voltage range. On the

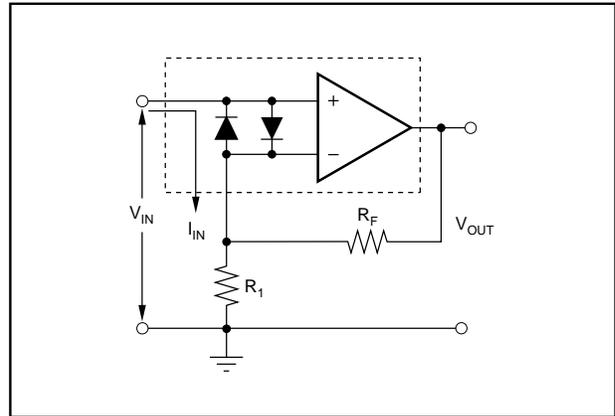


FIGURE 6. Current Path Through the Protection Diodes.

other hand, in this multiplexer configuration, a current flows through  $R_1$  and  $R_F$ , as shown in Figure 6. The voltage error from this current, which arises at the source, is also gained by a factor of 10. This error current disappears when input voltage steps are less than 0.7V, which is lower than the response threshold of the protection diodes.

### ELIMINATING ERROR

The voltage change at the filter capacitor is a product of the error current, the settling time, and the size of  $C_1$ . If  $R_F$  is selected ten times larger, the error decreases by about 1/10 to 1.2mV. For high-resolution converters, this error is still too large, and an  $R_F$  of 100k $\Omega$  is also a significant error source for bipolar op amps. On the other hand, it is also possible to enlarge  $C_1$ , although the mechanical dimensions of 1 $\mu$ F to 4.7 $\mu$ F set a limit to the value of capacitor selected. A compromise of  $C_1 = 2\mu$ F and  $R_F = 25k\Omega$  produces an acceptable error of about 0.3mV, based on a 10V voltage difference between the channels and a circuit as shown in Figure 5.

If, however,  $R_1$  and  $C_1$  are significantly decreased to enable recharging from the source, the effect of the low-pass filter and its protection decrease greatly. Even more important, the current pulse in this case would flow across the supply line between the source and the filter input, which is undesirable for other reasons.

The error current can also be reduced using a current-limiting circuit. This type of circuit is described under the section "Tips". For better error elimination, a FET op amp can be used. As already mentioned, this op amp does not allow the error current to increase at all.

### INSTRUMENTATION AMPLIFIER

If the threshold voltage of the protection diodes is known, it is easy to calculate the overload input current of an op amp circuit. With instrumentation amplifiers (INAs), the input protection circuitry is not always recognizable.

Although an INA at the inputs allows large voltage differences, dynamic overload at first produces the same error currents as those using op amps. This problem is illustrated in Figure 7, which shows a discrete circuit using three op amps.

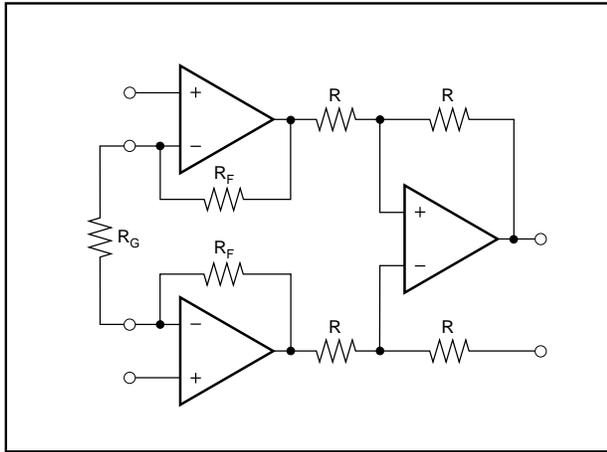


FIGURE 7. Instrumentation Amplifier.

In this configuration as well, the output of the input op amp can follow the input signal only with a finite slew rate. As described earlier, a current then flows through the protection diodes and  $R_F$ . This is true both for the common-mode voltages of the signal and for the differential signal itself. At small gains,  $R_G$  is high-impedance or is not present at all ( $G = +1V/V$ ). The error current then flows into the dynamically overloaded input.

In larger gain ranges,  $R_G$  becomes equal to or smaller than  $R_F$ . This factor can produce a current path to the other input, which could load the source there unexpectedly. Fortunately, the configuration is equipped with two diode paths in series which prevent signal and common-mode steps of less than 1V from producing such an error. In addition, common-mode steps produce a current in  $R_F$  but not in  $R_G$  since the voltage drop in both protection circuits is almost the same size so that there is no significant voltage change at  $R_G$ . This advantage is important, since especially during differential measurements using the multiplexer, common-mode voltage differences can arise, while the gain can be far above 100V/V with a correspondingly long settling time. The size of the error or the error current can then only be calculated if the input circuit and the resistances are known. This information is generally given in the data sheet.

### TIPS

As discussed in the section on op amps, the error current most often causes an error in measurement when a capacitive source is present or when a pulse-like current leads to errors in the signal source or the supply line. As already

mentioned, a FET INA such as the INA110 or INA111 prevents these error currents since no current path can arise if there are no protection diodes. In addition, the FET INA require no differential voltage protection circuitry.

One possible way to suppress error is to use a current limitation circuit placed in the input line of the sense amplifier. This circuit should either reduce the current as much as possible or allow the bias current of the amplifier to pass through with no voltage drop. This current limitation must also float with the signal and must cause no significant leakage currents when settled.

The first current limitation circuit considered here is a circuit using a J-FET. During settling, the FET circuit must reduce the current to a low value. After the amplifier has settled and the current has fallen to the bias current of a few nanoampere, the FET should return to its ohmic region. In this region, the FET has a resistance of several thousand ohm. At the bias current of a few nanoampere, the voltage drop would remain a few microvolts and thus come close to the desired effect.

One J-FET with extremely low  $I_{DDs}$  is the 2N4117A. The 2N4117A allows an  $I_{DDs}$  of 30 $\mu$ A to 90 $\mu$ A. In the ohmic region, with a current of only 2nA (equal to the bias current of the INA114 or PGA204), the channel resistance is about 10k $\Omega$  (see Figure 8).

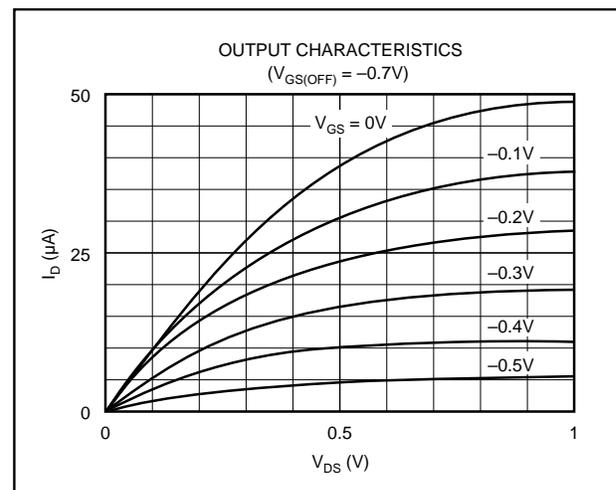


FIGURE 8. J-FET Characteristics.

This single current source, which is connected to the source at the gate, only operates for one polarity; otherwise, the gate-channel diode is conductive. For this reason, two FETs with opposite polarity are required for this configuration. This circuit limits the overload current to less than 90 $\mu$ A, certainly a great improvement over the 800 $\mu$ A mentioned earlier. In combination with the 1 $\mu$ F filter capacitor, the circuit reduces the error to approximately 0.1mV. The remaining settling time of an INA, however, is more like 15 $\mu$ s, producing approximately 0.5mV.

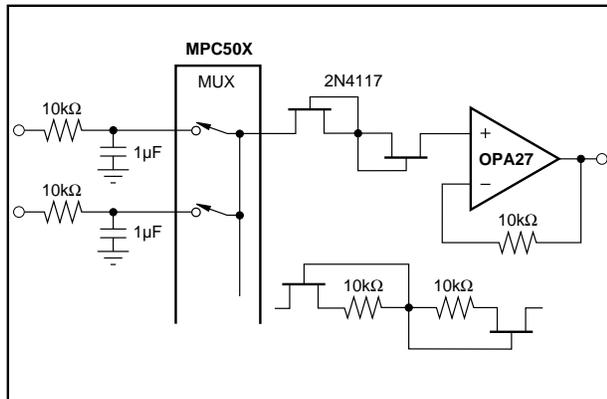


FIGURE 9. Current-Limiting Circuit Using a J-FET.

Using resistors in the source line of the FET circuit allows an even greater reduction of the current limitation. This reduction increases the total resistance in the supply line to the amplifier input. The FETs alone produce about  $10\text{k}\Omega + 10\text{k}\Omega$ . To go from the typical  $60\mu\text{A}$  to  $30\mu\text{A}$ , about  $10\text{k}\Omega$  are necessary in the source line (see Figure 9). Thus, if the error current was reduced by half, the total resistance would rise to  $40\text{k}\Omega$  and  $40\text{k}\Omega$  is an acceptable value for the error caused by the bias current. Larger values would cause bias current errors to exceed the offset errors.

Example:

Bias Current Drift: PGA204AP  $8\text{pA}/^\circ\text{C}$

Bias Resistance:  $40\text{k}\Omega$

$I_{OS}/^\circ\text{C} = 8\text{pA}/^\circ\text{C} \cdot 40\text{k}\Omega = 0.32\mu\text{V}/^\circ\text{C}$

Since the  $0.3\mu\text{V}/^\circ\text{C}$  is close to the  $0.25\mu\text{V}/^\circ\text{C}$  offset drift, the  $40\text{k}\Omega$  will not cause a significant error over temperature. The current limitation circuit described here can also be used as a protection circuit in front of the inputs. The isolation voltage strength is that of the FETs used. The current is limited to such a small value that the internal diodes to the semiconductor substrate is sufficient to redirect the current.

## MUX OUTPUT CAPACITANCE

The ON resistances of analog multiplexers can vary greatly and due to the protection circuitry, can amount up to  $2\text{k}\Omega$  (in this case, the protection circuitry is ohmic resistors). Another varying factor is the channel capacitance and, consequently, the capacitance that influences the output. This capacitance is switched from one channel to the next, is up to  $100\text{pF}$  per IC, and is, of course, dependent upon the number of channels and the desired on-resistance. At  $2\text{k}\Omega$  and  $50\text{pF}$ , the settling time constant is  $0.1\mu\text{s}$ . This constant is negligible for most applications, but as already discussed, it overloads most amplifiers.

This charge in the output capacitance also produces a current pulse to the signal source. If, as described above, the input is configured with the obligatory low-pass filter, the transferred charge flows into the filter capacitor, producing a charge compensation between the two capacitors that are now in parallel (see Figure 10). Simply the fact that an additional  $50\text{pF}$  filter capacitor is wired parallel to a  $100\text{nF}$  capacitor makes it probable that the former, at 2000 times the latter, will have a significant influence on it. Of course, this configuration does require a break-before-make; otherwise, further compensation and error currents arise. This break-before-make, however, can only be maintained within an IC. If several multiplexers are cascaded, problems can easily arise.

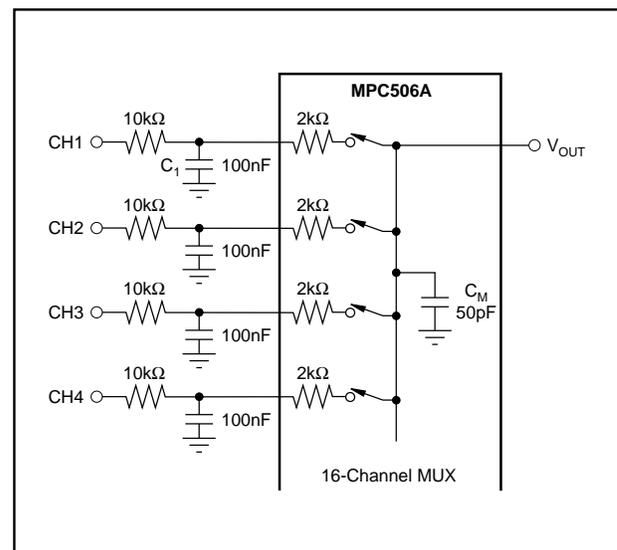


FIGURE 10. Mux Capacitance  $C_M$ .

As shown in the “normal” circuit in Figure 10, the influence of  $C_M$ , the multiplexer output capacitance, is easy to see.

Example:

In channel 1,  $C_M$  was charged to  $0\text{V}$ . After the switching,  $C_M$  is switched parallel to  $100\text{nF}$  ( $C_1$ ), which is charged to  $10\text{V}$ . The charge constant of  $2\text{k}\Omega$  and  $50\text{pF}$  is only  $100\text{ns}$ . In contrast, the recharge time constant from the source to  $C_1$  is  $1\text{ms}$ , thus significantly longer. Using simplification, the charge of  $C_M$  is switched parallel to the  $100\text{nF}$  capacitor.

$$Q_{C1} = 100\text{nF} \cdot 10\text{V}$$

$$Q_{CM} = 50\text{pF} \cdot 0\text{V}$$

$$Q_{C1} = Q_{CM} = 100\text{nF} \cdot 10\text{V} + 50\text{pF} \cdot 0\text{V}$$

$$V_2 = \frac{Q_{C1} + Q_{CM}}{C_1 + C_M} = \frac{1\text{E}^{-6}}{100\text{E}^{-9} + 50\text{E}^{-12}} = 9.99550\text{V}$$

$$V_1 = 10\text{V}$$

$$\Delta V = V_1 - V_2 = 4.5\text{mV Error Voltage}$$

This calculation is greatly simplified, but the filter time constant of 1ms causes the 4.5mV error to settle very slowly, while the conversion of the selected channel usually should begin after 100µs or less. For this reason, the error that arises in the conversion is described as crosstalk. In addition to the 50pF, the external capacitances from the conductors and the input capacitance of the succeeding amplifier also contribute to the error. The resulting total error exceeds the LSB threshold of a 12-bit converter. In the worst scenario, the preceding channel has -10V while its successor has +10V, in which case the deviation is already doubled.

These errors can be avoided by either a large  $C_1$  or a low-pass filter with a very short time constant. As already mentioned, a short time constant of a few microseconds will not always be able to produce the desired filter effect. An amplifier in front of the MUX input decouples the input filter and drives the multiplexer in low-impedance mode. This solution eliminates both dynamic overload of the amplifier after the MUX and error from the charge transmission. In addition, the amplifiers can also raise the signal amplitude and can be configured as active filters.

## SUMMARY

Fault currents in the input of the amplifier can be large enough to generate significant errors. Filters at the input of a data acquisition multiplexer are practically unavoidable, yet they can also become a significant source of error. Great stress is thus placed on the parameters of the sense amplifiers succeeding the multiplexer, especially in high-resolution systems. The protection circuitry described here with two FETs is especially recommended for programmable gain amplifiers (PGAs) since the circuitry of these amplifiers often produces large overload input currents that can only be limited externally.

For large signals, amplifiers with FET inputs allow easy error reduction. Modern FET op amps and INAs now offer very good DC stability and low voltage noise, making them preferable to bipolar amplifiers in many applications.